Amendments to the Claims:

Please amend the claims as follows:

Claims 1-7 (Canceled).

Claim 8 (Currently Amended): A method of manufacturing a semiconductor device comprising:

a first step of forming an insulating film on a substrate;

a second step of forming a stacked substrate having a stacked layer of a first semiconductor layer and a second semiconductor formed on the first semiconductor layer;

a third step of bonding the substrate and the stacked substrate such that the insulating film faces the first semiconductor layer;

a ~~forth~~ fourth step of removing the stacked substrate so as to allow the first semiconductor layer and at least part of the second semiconductor layer to remain, thereby forming a stacked structure formed of the first semiconductor layer lattice-relaxed and the second semiconductor layer having a strain applied on a surface thereof; and

a fifth step of forming a transistor on the second semiconductor layer having a strain applied on the surface thereof.

Claim 9 (Original): The method according to claim 8, wherein the fifth step includes the steps of:

forming a gate insulating film selectively on an upper surface of the second semiconductor layer;

doping impurities for forming a channel region into an upper surface of the second semiconductor layer immediately under the gate insulating film;

forming a gate electrode on the gate insulating film; and

doping impurities selectively into the second semiconductor layer along opposite sides of the gate electrode with the gate electrode used as a mask, thereby forming a pair of source/drain regions.

Claim 10 (Original): The method according to claim 8, wherein the second step includes a step of controlling a thickness of the first semiconductor layer to 80 nm or less.

Claim 11 (Original): The method according to claim 8, wherein the fourth step includes a step of controlling a total thickness of the first semiconductor layer and the at least part of the second semiconductor layer to 100 nm or less.

Claim 12 (Original): The method according to claim 8, wherein the second step includes a step of forming the first semiconductor layer while varying a lattice distance in a film-thickness direction.

Claim 13 (Original): The method according to claim 8, wherein the first semiconductor layer and the second semiconductor layer are an SiGe layer and an Si layer, respectively, and the second step includes a step of controlling a Ge content of the first semiconductor layer at least at a portion thereof adjacent to the second semiconductor layer at more than 30 atomic %.

Claim 14 (Original): The method according to claim 8, wherein the first semiconductor layer and the second semiconductor layer are an SiGe layer and an Si layer,

respectively, and the second step includes a step of controlling a Ge content to have a gradient content in such a manner that a Ge content of a portion of the first semiconductor layer adjacent to the insulating layer is set at 30% or less and a Ge content of a portion of the first semiconductor layer adjacent to the second semiconductor layer is set at more than 30 atomic %.

Claim 15 (Currently Amended): A method of manufacturing a semiconductor device comprising:

a first step of forming an insulating film on a substrate;

a second step of forming a first semiconductor layer on a surface of a semiconductor substrate;

a third step of bonding the substrate and the semiconductor substrate such that the insulating film faces the first semiconductor layer;

a ~~forth~~ fourth step of removing the semiconductor substrate so as to leave at least the first semiconductor layer, thereby lattice-relaxing the first semiconductor layer;

a fifth step of stacking a second semiconductor layer on the first semiconductor layer, thereby applying a tensile strain to the second semiconductor layer; and

a sixth step of forming a transistor on the second semiconductor layer.

Claim 16 (Original): The method according to claim 15, wherein the sixth step includes the steps of:

forming a gate insulating film selectively on an upper surface of the second semiconductor layer;

doping impurities for forming a channel region into an upper surface of the second semiconductor layer immediately under the gate insulating film;

forming a gate electrode on the gate insulating film; and

forming a pair of source/drain regions by doping impurities selectively in the second semiconductor film along opposite sides of the gate electrode with the gate electrode used as a mask.

Claim 17 (Original): The method according to claim 15, wherein the fourth step includes a step of controlling a thickness of the first semiconductor left to 80 nm or less.

Claim 18 (Original): The method according to claim 15, wherein the fifth step includes a step of controlling a total thickness of the first semiconductor layer and the second semiconductor layer to 100 nm or less.

Claim 19 (Original): The method according to claim 15, wherein the second step includes a step of varying a lattice distance of the first semiconductor layer in a film thickness direction.

Claim 20 (Original): The method according to claim 15, wherein the first semiconductor layer and the second semiconductor layer are in an SiGe layer and an Si layer and the second step includes a step of setting a Ge content of a part of the first semiconductor layer at least adjacent to the second semiconductor layer at more than 30 atomic %.

Claim 21 (Original): The method according to claim 15, wherein the first semiconductor layer and the second semiconductor layer are an SiGe layer and an Si layer, respectively, and the fourth step includes a step of controlling a Ge content to have a gradient content in such a manner that a Ge content of the first semiconductor layer a portion thereof adjacent to the insulating layer is set at 30 atomic % or less and a Ge content of a surface of the first semiconductor layer exposed to air is set at more than 30 atomic %.

Claim 22 (Canceled).